IN THE SPECIFICATION:

Please amend the paragraph beginning at page 10, line 24, as follows:

--If the eject command arrives, the control circuit 10 invalidates the ATA interface circuit 11 in step S102 in order not to receive a subsequent command. At this time, the ATA interface circuit 11 may be invalidated by hardware, or some or all of incoming commands may be ignored by software processing of the control circuit 10. In step S103, the control circuit 10 waits for the end of predetermined operation of the hard disk drive 20. More specifically, when the RAM element in the control circuit 10 is used as a write cache memory, the control circuit 10 waits until the cache is ~~flashed~~ flushed (cache contents are written in the magnetic storage medium 16). When the removable hard disk cartridge 1 is ejected after rotation of the platter 16 ends, the control circuit 10 waits for the end of rotation stop processing. These are merely examples. In any case, in step S103, the control circuit 10 waits for the end of various operations which should be executed before the removable hard disk cartridge 1 is ejected. After the end of predetermined operation, the eject signal is set low in step S104. Although not particularly illustrated in FIG. 3, the state may shift to a SLEEP mode defined by ATA interface standards after step S104.--